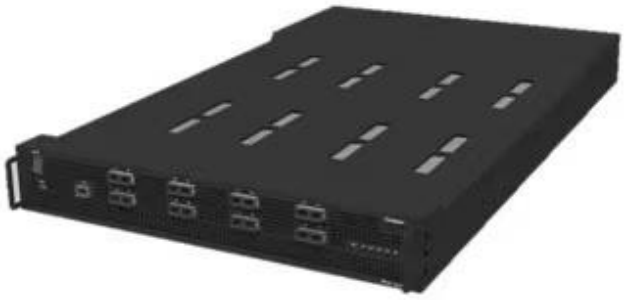
MIMIC FPGA PROTOTYPING SYSTEM

For Fastest ASIC Prototyping and Debugging

The Corigine MIMIC Prototyping System is a high-performance, FPGA-based system that raises prototyping to an unprecedented new level. The MIMIC system enables early software development, system validation and regression testing, while significantly reducing development time and workload.



Corigine MIMIC Prototyping System (4-FPGA)

Corigine MIMIC FPGA Prototyping System

The Corigine MIMIC Prototyping System provides performance and speed for ASIC and software development for both enterprise and cloud operation, with utmost security and scalability.

DEVELOPMENT ACCELERATION

The Corigine MIMIC system is the industry's next-generation platform for automating prototyping including partitioning operations, while providing a system-level view for optimum partitioning and performance. In addition, the MIMIC system adds deep local debug capabilities providing much greater visibility and faster elimination of bugs. Thus the MIMIC system reduces the overall development time while also enabling early software development without the need for costly emulation.

SCALABILITY

The Corigine MIMIC system provides modular upgrabiliy for the prototyping of an enterprise's ASICs family of AI, Processor, Vision, Communication and other SOCs. The MIMIC solution provides scalability from 1 to 32 FPGAs. The system also provides easy upgrability to the latest available FPGAs.

CLOUD ACCESS & SECURITY

The Corigine MIMIC system has been architected for opration in both the Enterprise and Cloud environments. Also, the design enables security of the user IP thru encrypted prototyping.

Corigine MIMIC Prototyping System Key Features and Benefits:

Features	Benefits
Local Debug and System Scope Logic Analyzer	Provides high visibility for faster logic debug to quickly resolve bugs
System-Level Routing	Delivers highest system performance for software development thus reducing development time
Auto-Partitioning	Reduces manual intervention and R&D workload with automated pin-muxing and instrumentation
User Design Import	Supports both RTL Verilog and System Verilog as well as gate level EDIF
Automatic Clock Handling	Eliminates manual handling of gating clock thus reducing engineering workload and manual errors
Incremental Compilation	Minimizes compilation time
Memory Compiler/Analyzer	Eliminates time consuming recompilation by providing backdoor runtime memory access
Fault Injection	Force/Release capability, supporting automotive safety requirements
Vector Mode	Enables remote cloud deployment based on simulation stimulus

Specifications:

- Performance: 120MGates at an unprecedented performance level
- Scalable: 30 million to 1 billion gates (1 to 32 FPGAs)
- Built-in Memory analyzer, Memory compiler
- Parallel synthesis, parallel place and route
- Timing driven auto-partitioning
- Automated gated-clock conversion
- System scope with local memory for debug
- Fault injection, Force/Release for safety
- Runtime control for clock generation circuit
- Vector mode enabling cloud deployment and regression testing
- Built-in monitor and readback for all design flip-flops
- FMC interface boards: HDMI, USB, SD,UART, JTAG, SPI-Flash, DDR4

Corigine MIMIC Prototyping System (1-FPGA)